



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT : Seung-Hwan Oh
SERIAL NO. : 09/473,846 EXAMINER : Anne L. Damiano
FILED : December 28, 1999 ART UNIT : 2114
FOR : METHOD FOR PROCESSING ERROR OF RECEIVED PACKET IN
ETHERNET MAC LAYER

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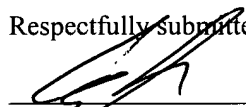
Dear Sir:

Appellants respectfully submit three copies of a Reply Brief For Appellants that includes an Appendix with the pending claims. The Reply Brief is now due on January 15, 2005.

In the event that any additional fee is required to continue the prosecution of this Application as requested, please charge such fee to Deposit Account No. 502-470.

Should the Examiner deem that there are any issues which may be best resolved by telephone communication, kindly telephone Applicants undersigned representative at the number listed below.

Respectfully submitted,


By: Steve Cha
Attorney for Applicant
Registration No. 44,069

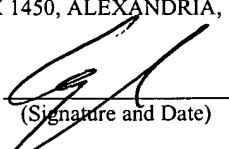
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor : Seung-Hwan Oh
Application No. : 09/473,846
Filed : December 28, 1999
For : METHOD FOR PROCESSING ERROR OF
RECEIVED PACKET IN ETHERNET MAC LAYER

REPLY BRIEF

On Appeal from Group Art Unit 2114

Date: 1/3/05

Steve Cha
Attorney for Applicant
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Steve S. Cha, Reg. No. 44,069
(Name of Registered Representative)

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TABLE OF CONTENTS

	<u>Page</u>
I. REAL PARTY IN INTEREST.....	3
II. RELATED APPEALS AND INTERFERENCES.....	3
III. STATUS OF CLAIMS.....	3
IV. STATUS OF AMENDMENTS.....	3
V. SUMMARY OF THE INVENTION.....	3
VI. ISSUES.....	3
VII. GROUPING OF CLAIMS.....	4
VIII. ARGUMENT.....	6
IX. CONCLUSION.....	14
X. APPENDIX: THE CLAIMS ON APPEAL.....	15

I. REAL PARTY IN INTEREST

The appellant relies on the content of the appeal brief.

II. RELATED APPEALS AND INTERFERENCES

The appellant relies on the content of the appeal brief.

III. STATUS OF CLAIMS

The appellant welcomes the substitution, as indicated in the Examiner's Answer, of the claims in the June 29, 2004 amendment, claims 1-4, to replace the claims 1-4 of record at Final Rejection.

IV. STATUS OF AMENDMENTS

The appellant welcomes the substitution, as indicated in the Examiner's Answer, of the claims in the June 29, 2004 amendment, claims 1-4, to replace the claims 1-4 of record at Final Rejection.

V. SUMMARY OF THE INVENTION

The appellant relies on the content of the appeal brief.

VI. ISSUES

The appellant relies on the content of the appeal brief.

VII. GROUPING OF CLAIMS

The Examiner's Answer challenges the grouping of claims set forth in the appeal brief, but the appellant traverses this challenge.

The appeal brief states, in section 6 ("ISSUES"), that: claims 2 and 3 stand or fall together; claim 1 stands or falls separately; and claim 4 stands or falls separately. 37 CFR 1.192(c)(7) provides:

For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together

In the instant case, based upon the "ISSUES" section of the Examiner's Answer (section 6), the Examiner's Answer concurs with the appeal brief that claims 2 and 3 are subject to a different ground of rejection than claim 1. Likewise, the Examiner's Answer concurs that the ground of rejection for claims 2 and 3 differs from that of claim 4. In effect, each of the claim groupings, i.e., 2 and 3; 1; and 4 is subject to a separate ground of rejection.

The Examiner's Answer apparently does not recognize this concurrence, due to its seeming misconception regarding what is meant by the phrase "ground of rejection."

Referring, for example, to the MPEP:

For example, if claims 1 to 4 are rejected under 35 U.S.C. 102 and appellant considers claim 4 to be separately patentable from claims 1 to 3, he or she should so state in the "Grouping of claims" section of the brief, and then give the reasons for separate patentability in the 35 U.S.C. 102 portion of the "Argument" section (i.e., under 37 CFR 1.192(c) (8) (iii)). MPEP 1206 (7).

In accordance with 37 CFR 1.192(c)(7), the Board can select a single one of claims 2 and 3 of the present patent application to decide patentability of the group of claims comprised of claims 2 and 3.

The Examiner's Answer suggests, by contrast, that the rejection of claims 2 and 3 stands or falls together with the rejection of the other claims, i.e., claims 1 and 4. As authority for this proposition, the Examiner's Answer cites 37 CFR 1.192(c)(7).

However, as set forth above, the statement by the appellant of the ISSUES in section VII of the appeal brief, when properly interpreted under 37 CFR 1.192(c)(7), leads to the conclusion that claims 2 and 3 stand or fall together and that each of claims 1 and 4 stands or falls alone.

In addition, the Examiner's Answer incorrectly suggests that the appeal brief fails to include "reasons" to support separate patentability.

Firstly, however, the reasons are required only when separate consideration is requested for individual claims subject to the same ground of rejection. This situation, however, does not apply in the instant patent application.

Secondly, the reasons may "be included in the appropriate portion of the 'Argument' section of the brief" MPEP 1206 (7).

We believe that, as between the separate claim groupings, the appellant's analysis is sufficiently well-developed in the "Argument" section as to make clear the separate reasons for patentability.

For at least all of the above reasons, the appellant submits that the challenge in the Examiner's Answer to our claim groupings lacks foundation and is without merit.

VIII. ARGUMENT

A. CLAIM REJECTIONS UNDER 35 U.S.C. 102(e)

Claim 1, as now acknowledged by the Examiner's Answer in section (3), "Status of Claims," recites:

receiving a packet from the physical layer and transmitting the packet to a switch; detecting for an error while transmitting the packet; upon detection of the error, stopping the transmission of the packet in which the error is detected to the switch without waiting for a complete reception of the entire packet in which the error is detected; and transmitting a signal indicating an occurrence of the error and a signal indicating an end of the packet to the switch

Firstly, Haddock fails to disclose or suggest, "stopping the transmission of the packet in which the error is detected to the switch without waiting for a complete reception of the entire packet in which the error is detected," which language explicitly appears in the present claim 1.

Until the Examiner's Answer, the Examiner fails to cite to Haddock, or offer explanation, as to what in Haddock is deemed to correspond to the second clause of the above quote, i.e., "without waiting for a complete . . ."

The Examiner's Answer now offers the next-to-last sentence of the last full paragraph on page 5, which states, "When the MAC is transmitting to another node, it is receiving the packet from the Physical layer for transmission."

The appellant traverses this statement on page 5 of the Examiner's Answer.

As acknowledged in the first sentence of the second full paragraph on page 5 of the Examiner's Answer, Haddock relies on the carrier sense multiple access/collision

detection (CSMA/CD) protocol. Haddock pertains to CSMA/CD on a local area network (LAN) (“Field of the Invention”; first sentence: col. 1, lines 21-26).

CSMA/CD is a “listen” and “send” access method, implemented on a shared communication medium (Haddock, col. 1, lines 42-44). An Ethernet data packet (Haddock, col. 1, lines 52-53: “Ethernet data packets”) is sent on the medium, that packet including a source address and a destination address, the latter two identifying, respectively, the transmitting node and the receiving node.

Just prior to sending a packet, the potentially sending node “listens” to the medium to determine whether the medium is busy, i.e., whether another node of the LAN is currently sending data on the medium. In particular, to make this determination, the node is “listening” for the presence or non-presence of a carrier signal on the medium (Haddock, col. 6, lines 36-39).

If the potentially sending node detects the medium as being busy, the potentially sending node does not send the packet.

On the other hand, if the potentially sending node detects the medium as being idle, the potentially sending node sends the packet.

In particular, “all nodes are peers such that only one node may successfully transmit a data packet at a time” (Haddock, col. 2, lines 13(14)-15(16)).

The moment after any node starts transmitting its data packet, any other node detecting whether the medium is busy or idle will determine that the medium is busy. Thus, the node that is sending the packet has exclusive access to the medium while transmitting its packet.

The exception to the above rule of exclusive transmission access is an unsuccessful transmission due to a collision. If two or more nodes on the LAN simultaneously attempt to send their respective packet, e.g., due to each having just detected the medium to be idle, a collision will result (Haddock, col. 6, lines 49-50). The collision is what the Examiner characterizes as introducing an error in the packet being transmitted. Each of the colliding nodes detects the collision by sensing it on the medium, and stops transmitting its respective packet. CSMA/CD later resolves priority between among the colliding nodes. This sensing, by a colliding node, of the collision and, in response, stopping its transmission of its packet is what the Examiner's Response characterizes as "stopping the transmission of the packet in which the error is detected" in the present claim 1 (Examiner's Answer, page 5, third full paragraph, first sentence).

Returning now to the Examiner's statement in the next sentence, "When the MAC is transmitting to another node, it is receiving the packet from the Physical layer for transmission," this statement appears to be saying that when the MAC layer of a node A is transmitting a packet to a node B, the MAC layer of node A is receiving the packet from the physical layer for transmission.

However, as set forth in the analysis above, while a node A on the LAN is receiving a packet, another node, B, on the LAN, i.e., the sending node, has exclusive transmission access on the LAN. Nodes A and B cannot be the same, at least since the destination address a node inserts into a packet, to prepare the packet for transmission, cannot be the address of the node itself. Since node B has exclusive transmission access, node A cannot be transmitting. Accordingly, for at least this reason, node A cannot concurrently be receiving and transmitting a given packet.

Moreover, reception of the packet at a given node would prevent its transmission from the given node from concurrently occurring, at least because the node would detect the medium as being busy by virtue of the carrier signal on which the packet is being received and, in response, refrain from transmitting.

In particular, Haddock fails to disclose or suggest, “stopping the transmission of the packet in which the error is detected to the switch without waiting for a complete reception of the entire packet in which the error is detected,” which language explicitly appears in the present claim 1.

In addition, all of the analysis in the appeal brief regarding the instant rejection of claim 1 continues to apply, and addresses other shortcomings in Haddock with regard to the instant rejection of claim 1. The substitution of the language “packet in which the error is detected” for “error packet,” noted in section 3 of the Examiner’s Answer and mentioned above in this section, does not appear to change the analysis set forth in the appeal brief.

The “Response to Argument” section, section 11, of the Examiner’s Answer incorrectly suggests that the appeal brief intends to show detecting is occurring on the physical layer (Examiner’s Answer: the paragraphs bridging pages 9 and 10 and pages 10 and 11). A careful reading of the analysis in the appeal brief shows, however, no such intention. The analysis instead demonstrates how it cannot fairly be said that Haddock discloses or suggests the first step of claim 1.

Returning to this latter point, the first step of claim 1 recites, “receiving a packet from the physical layer and transmitting the packet to a switch.”

The last sentence of the first paragraph of the “Response to Argument” section, section 11, of the Examiner’s Answer characterizes “another node” as being the switch of the present claim 1. Also, as set forth above, the Examiner characterizes the detecting step of the present claim 1 as being performed by a sending node that is contending for exclusive transmission access to the medium (Examiner’s Answer, page 5, third full paragraph, first sentence). In the detecting step of claim 1, “the packet” refers back to “a packet” in the preceding receiving and transmitting step.

Based on the above, the appellant can draw no other conclusion but that the Examiner sees the “transmitting” of claim 1 as being performed in Haddock by a sending node contending for exclusive transmission access, and sees the recipient “switch” of claim 1 as being “another node” in Haddock.

However, the transmission of a packet from a sending node to “another node” occurs at the physical layer, which is the lowest layer. Transmitting a packet at the physical layer can occur only as a direct result of receiving the packet from an upper layer, i.e., a layer above the physical layer. This contradicts the language of claim 1, “receiving a packet from the physical layer and transmitting the packet to a switch.”

It appears that the remainder of the “Response to Argument” section of the Examiner Answer, with respect to the present claim 1, has been adequately traversed, and therefore nothing further need be said.

For at least all of the above reasons, Haddock fails to anticipate the invention as recited in claim 1.

B. CLAIM REJECTIONS UNDER 35 U.S.C. 103(a)

1. Rejection of claims 2 and 3

As a preliminary matter, the appellant notes that the “Grounds of Rejection” section of the Examiner’s Answer, section 10, incorrectly characterizes, on page 6, the instant rejection as being anticipatory. As section 6 of the Examiner’s Answer already acknowledges, however, the instant rejection attempts to rely on 35 U.S.C. 103.

Claim 2, as now acknowledged by the Examiner’s Answer in section (3),

“Status of Claims,” recites:

A method for processing a packet exceeding a predetermined size received from a physical layer by a MAC layer of an Ethernet, wherein the received packet is stored in a memory for an eventual transmission to a switch, the method comprising the steps of:
receiving a packet from the physical layer, storing the received packet in the memory, and transmitting the received packet to the switch;
detecting for error while receiving the packet;
upon detection of the error, stopping the storage of the packet in which the error is detected in the memory and the transmission of the packet in which the error is detected to the switch without waiting for a complete reception of the packet in which the error is detected; and,
transmitting a signal indicating an occurrence of the error and a signal indicating an end of the received packet to the switch

The first point raised in the appeal brief, in response to the instant ground of rejection, is “Firstly, the only stopping mentioned in the PAAA applies to a packet not exceeding 64 bytes in length, i.e., a short packet, but the PAAA does not disclose or suggest that a short packet is sent to a switch.”

In purported response, the Examiner’s Answer suggests that “transmitting to a node includes such scenario of transmitting to a switch” (page 11, last paragraph). In other words, the Examiner’s Answer is, for this ground of rejection, making the same argument

it presents for the previous ground of rejection, i.e., that if it has to find a “switch” out there somewhere in the network that is no problem and it won’t worry about it.

Since, however, the present claim 2 recites, “A method for processing a packet . . . received from a physical layer by a MAC layer of an Ethernet,” it appears somewhat awkward to be searching out other nodes of the network for a “switch.”

Moreover, since the Examiner has chosen to use, as the primary reference, the prior art version of processing a packet received from a physical layer by a MAC layer of an Ethernet, the applicants do not believe refuge can properly be found in other nodes of the network.

In this context, the appellant refers to the first paragraph on page 12 of the Examiner’s Answer. Firstly, to avoid the problem of not being able to make the claim rejection based on the assumption of a larger packet (appeal brief, page 11, 3rd full paragraph), the Examiner’s Answer maintains the stance that the “examiner has asserted a predetermined size of 1 byte (page 11, second full paragraph). Then, the above-referenced first paragraph of page 12 of the Examiner’s Answer states, “When the MAC starts forwarding a packet before the entire packet is received . . .” Presumably, then, the packet being forwarded by the MAC “before the entire packet is received” is a short packet. Problematically, however, the PAAA makes no such disclosure or suggestion of the MAC “forwarding” a short packet before the entire packet is received. The Examiner’s “fiction” of such disclosure apparently amounts to an attempt to find non-existent motivation (appeal brief, starting at first full paragraph on page 12) for modifying the PAAA to feature, “transmitting a signal indicating an occurrence of the error and a signal indicating an end of the received packet to the switch.”

Further with regard to the Examiner's incorrect suggestion that the PAAA discloses sending short packets to the switch (Examiner's Answer, page 6, second full paragraph), the Examiner cites lines 5-6 of page 2 of the instant specification, but reference to the cited passage reveals no such disclosure or suggestion.

The Examiner then says that the "Examiner believes there are no deficiencies in claim 2" (Examiner's Answer, page 12, last paragraph). The appellant notes this, while realizing the Examiner probably intends to say that there are no deficiencies in the Examiner's arguments.

The appellant believes that, even in view of the Examiner's Answer, the other arguments presented by the Examiner as to this ground of rejection have been adequately traversed in the appeal brief.

Claim 3 depends from claim 2, and is deemed patentable over the cited references for at least the same reasons set forth above with regard to claim 2.

2. Rejection of claim 4

The appellant relies on the content of the appeal brief.

IX. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Respectfully submitted,

Steve S. Cha
Registration No. 44,069



Attorney for Applicant

Date: 1/3/05

X. APPENDIX: THE CLAIMS ON APPEAL

1. A method for processing a packet exceeding a predetermined size received from a physical layer by a MAC (Medium Access Control) layer of an Ethernet to be transmitted to a switch, the method comprising the steps of:

receiving a packet from the physical layer and transmitting the packet to a switch;

detecting for an error while transmitting the packet;

upon detection of the error, stopping the transmission of the packet in which the error is detected to the switch without waiting for a complete reception of the entire packet in which the error is detected; and

transmitting a signal indicating an occurrence of the error and a signal indicating an end of the packet to the switch.

2. A method for processing a packet exceeding a predetermined size received from a physical layer by a MAC layer of an Ethernet, wherein the received packet is stored in a memory for an eventual transmission to a switch, the method comprising the steps of:

receiving a packet from the physical layer, storing the received packet in the memory, and transmitting the received packet to the switch;

detecting for error while receiving the packet;

upon detection of the error, stopping the storage of the packet in which the error is detected in the memory and the transmission of the packet in which the error is detected

to the switch without waiting for a complete reception of the packet in which the error is detected; and,

transmitting a signal indicating an occurrence of the error and a signal indicating an end of the received packet to the switch.

3. The method as claimed in Claim 2, wherein the method further comprising the step of preparing to receive a next packet from the physical layer after receiving the packet in which the error is detected.

4. The method as claimed in Claim 2, wherein said memory comprises a FIFO (First-In, First-Out) memory.